

(19)



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Office européen des brevets



35

(11)

EP 0 367 458 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
05.06.1996 Bulletin 1996/23

(51) Int Cl.⁶: **H03F 1/32**

(21) Application number: 89310827.4

(22) Date of filing: 20.10.1989

(54) **A predistortion compensated linear amplifier**
Vorverzerrungskompensierter linearer Verstärker
Amplificateur linéaire à précorrection de distribution

(84) Designated Contracting States:
DE FR GB NL SE

(30) Priority: 31.10.1988 US 265187

(43) Date of publication of application:
09.05.1990 Bulletin 1990/19
✓

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Description

This invention relates to distortion compensation circuits.

RF linear amplifiers utilize devices that exhibit non-linear characteristics at higher power levels whereby signal distortion is introduced. If more than one signal is applied to an RF amplifier, its non-linear characteristics cause an unwanted multiplicative interaction of the signals being amplified and the amplifier output contains intermodulation products. These intermodulation products cause interference and crosstalk over the amplifier frequency operating range which interference may exceed established transmission standards.

As is well known, intermodulation distortion can be reduced by predistorting the signal to be amplified to cancel the amplifier generated distortion. Some predistortion techniques such as described in U. S. Patent 4,465,980 use non-linear elements to compensate for the distortion generated in the amplifier. The characteristics of the non-linear elements, however, generally differ from those of the amplifier to be corrected so that compensation is only effective over a limited range. Other arrangements such as described in U. S. Patent 4,291,277 or U. S. Patent 4,554,514 utilizes the base band converted modulation component of one input signal to produce predistortion but is not effective for systems having a plurality of concurrent signals or over an extensive range of frequencies.

U. S. Patent 3,755,754 describes a predistortion compensation arrangement for a microwave amplifier in which a multifrequency signal is applied to a power amplifier through a variable phase shifter and through a distortion producing amplifier having substantially similar distortion transfer characteristics. The output of the distortion producing amplifier is combined with the undistorted signal from the variable phase shifter to form a predistortion signal having distortion components opposite in phase to the distortion components of the power amplifier whereby compensation is obtained. In similar fashion, U. S. Patent 4,068,186 discloses a circuit for compensating for non-linear characteristics in high frequency amplifiers in which an input signal is divided into two parts. One part is applied to a first transmission line having a delay line and the other part is applied to a second transmission line having a distortion producing high frequency amplifier. The vector sum of the transmission line outputs provides a non-linear characteristic that compensates for amplitude and phase non-linear characteristics of a high frequency amplifier connected in cascade with the compensating circuit. While the use of a distortion generating amplifier with similar distortion characteristics to the amplifier to be corrected provides a significant improvement, the control of the predistortion circuits is preset so that variations in circuit element characteristics due to changes in operating conditions may adversely affect distortion compensation.

U.S. Patent 4,453,133 discloses an active predis-

torter for linearity compensation which also utilizes distortion characteristics of an amplifier similar to the power amplifier to be corrected. An input signal is divided into a part that is applied to a signal path having a linear delay, a part that is applied to the distortion producing amplifier and a part that is combined with a portion of the output of the distortion producing amplifier to generate a phase inverted predistortion signal. The phase inverted predistortion signal is combined with the linear delay path signal and applied to the input of the amplifier to be corrected. Optionally, a portion of the power amplifier output signal is feedback to provide a closer match in the operating characteristics of the amplifier to be corrected and the distortion producing amplifier. This arrangement, however, results in attenuation of the input signal through the predistortion circuit and does not provide continuous control of the attenuation and phase characteristics needed for distortion compensation. According to the invention the operation of a predistortion type linearity compensator is improved by using an incoming carrier signal to control distortion removal thereby providing accurate distortion compensation while allowing full use of a wide band frequency range.

U.S. patent 4,560,945 discloses an adaptive feed forward cancellation system employing modulators to control the phase and amplitude of cancellation signals used for reducing distortion and intermodulation product signals of a bank of power amplifiers. To prevent coupling of these signals through the modulators to the output of the amplifier, the modulators are connected to the inputs of the bank of power amplifiers.

U.S. patent 4,394,624 discloses an amplification system for processing multiple channels over a wide frequency range. Feed forward techniques are utilized to reduce distortion products in the amplifier output. Distortion reduction is enhanced by treating individual channels of frequency sub-bands of the multi channel signal being processed to reduce the signal distortion.

According to this invention there is provided a distortion compensation circuit according to claim 1.

Distortion may be removed from the power amplifier output by detecting an intermodulation distortion signal thereat, monitoring the intermodulation distortion signal and adjusting the magnitude and phase of the output of the first combining means to minimize the monitored intermodulation distortion signal.

Brief Description of the Drawing

FIG. 1 depicts a block diagram of a distortion compensating circuit illustrative of the invention; FIG. 2 shows a more detailed block diagram of the controller of FIG. 1; FIGS. 3, 4 and 5 are flow charts illustrating the operation of the controller of FIG. 2; FIG. 6 depicts a block diagram of another distortion compensating circuit illustrative of the invention; FIG. 7 is a flow chart illustrating the operation of the

controller of FIG. 6; and
FIG. 8 shows waveforms illustrating the operation
of FIGS. 1 and 6.

Detailed Description

FIG. 1 depicts a distortion compensation arrangement for a power amplifier operative to amplify signals across a prescribed frequency band that is illustrative of the invention. In FIG. 1, the power amplifier comprises a plurality of substantially identical amplifiers 135-1 through 135-N connected in parallel. Each of these amplifiers receives its input from combiner 115 via multiple output splitter 132. The outputs of amplifiers 135-1 through 135-N are combined into a single high power signal in multiple input combiner 137. Since the amplifiers are substantially identical, each has the same prescribed distortion characteristic. The circuit of FIG. 1 includes a predistortion amplifier 105 which is substantially identical to amplifiers 135-1 through 135-N and therefore has the same distortion characteristic. Compensation is obtained by isolating the distortion component of the output of amplifier 105 and applying a phase inverted version of the distortion to the inputs of amplifiers 135-1 through 135-N. The distortion compensation arrangement provides amplification of the one or more input signals applied thereto while adjusting the parameters to optimize the distortion compensation.

Referring to FIG. 1, a composite input signal s is split into two portions s_1 and s_2 in signal splitter 101. Portion s_1 is applied a first circuit path including amplifier 105. This amplifier provides a preset gain while inserting the prescribed distortion and supplies its output to directional coupler 110. The main output of coupler 110 is delayed in fixed delay element 113 and coupled therefrom to one input of combiner 115. Portion s_2 is applied to a second circuit path including gain and phase adjuster 103. Signal s_2 is modified by gain and phase adjuster 103 and applied to combiner 117 wherein a portion of the output of directional coupler 110 is combined with the modified signal s_2 to minimize signals other than a component corresponding to the distortion output of amplifier 105. If the amplitude and the phase of the signal from gain and phase adjuster 103 are properly adjusted, the amplified signal from directional coupler 110 is canceled by the clean signal from delay 104 so that only the prescribed distortion appears as the output of combiner 117. Splitter 120 supplies a portion of the output of combiner 117 on lead 142 to a control arrangement including controller 150 to control the parameters of gain and phase adjuster 103 as will be described.

The output of splitter 120 is applied to gain and phase adjuster 123 via lead 147. The modified distortion signal from adjuster 123 is inverted and amplified in voltage amplifier 127 by a preset amount and applied to an input of combiner 115. Adjuster 123 is adapted to modify the magnitude and the phase of the distortion signal from combiner 117 so that the distortion component of

the signal from combiner 115 is equal to the prescribed distortion of amplifiers 135-1 through 135-N but inverted in phase. As a result of the operation of the distortion compensation arrangement, the distortion produced by amplifiers 135-1 through 135-N is canceled by the oppositely phased distortion signal applied to the inputs of these amplifiers from combiner 115. The time delay of fixed delay element 113 is set to compensate for differences in the delays between the alternative paths for the input signal and the parameters of adjuster 123 are controlled by monitoring the distortion output of the amplifiers at directional coupler 138 and modifying the adjuster parameters to minimize the distortion output of the paralleled amplifiers.

In order to assure that the output of combiner 117 is representative of the prescribed distortion, the signal from splitter 138 on lead 140 is sent through RF switch 145 to mixer 155. Controller 150 supplies a scan signal to the other input of mixer 155 so that the prescribed frequency range of the amplifier is scanned from its low end to its high end. When a carrier signal is detected, the scan is interrupted and the carrier frequency is held. RF switch 145 then connects the output of splitter 120 to mixer 155 via lead 142 so that the output of combiner 117 is monitored by narrow band receiver 160. Controller 150 is then operative to modify the parameters of gain and phase adjuster 103 to reduce the magnitude of the detected carrier in the signal appearing at the output of combiner 117. The parameter modification operations are repeated until either the magnitude of the monitored carrier signal is minimized or a preset number of modifications have been completed.

FIG. 8 illustrates the frequency band of the circuit of FIG. 1. Both carrier and intermodulation distortion signals occur within the band. Carrier signals shown in waveforms 801, 803 and 805 have amplitudes greater than -30 db and an intermodulation distortion product signal 807 has an amplitude between -30 and -60 db. Controller 150 is operative to scan output 180 from one end, e.g., f_L , of the prescribed frequency band of the circuit of FIG. 1 to locate carrier signal S_c (waveform 801). Once the carrier signal is located, the magnitude of the carrier signal from combiner circuit 117 is monitored by the controller via RF switch 145, mixer 155 and narrow band receiver 160 and the amplitude and phase parameters of amplitude and phase adjuster 103 are iteratively modified to drive the carrier signal component of the output of the combiner 117 to a minimum. This amplitude and phase adjustment assures that the output of combiner 117 has the maximum carrier signal reduction.

It is also necessary to minimize the intermodulation product component of the power amplifier output. The prescribed frequency band is again scanned from end f_L in FIG. 8 by connecting the output of splitter 138 to mixer 155 via lead 140 and RF switch 145 to detect the intermodulation product signal of waveform 807. Once the intermodulation product signal is found, the parameters of amplitude and phase adjuster 123 are iteratively

modified to minimize the intermodulation product signal appearing on lead 140 from directional coupler 138. Advantageously, it is not necessary to remove a portion of the prescribed frequency band from service in order to insert a pilot signal for distortion reduction.

Controller 150 is shown in greater detail in FIG. 2. The circuit of FIG. 2 comprises a signal processor arrangement such as the Intel type D87C51 microprocessor and includes control program store 205 and control processor 210, carrier and intermodulation signal store 215, input interface 203, output interface 235 and bus 218. Analog to digital converter 201 receives signals representative of the magnitude of signals from receiver 160 and converts the analog signal into a series of digital values. Control processor 210 operating in accordance with instructions stored in control program store 205 causes these digital values to be sent to store 215 via input interface 203 and bus 218. The processor also provides digital signals to digital to analog converters 220, 225, 230, 240 and 245 via bus 218 and output interface 235. The analog output of converter 220 is supplied to voltage controlled oscillator (VCO) 152 to direct scanning operations. The output of converters 225 and 230 are sent to amplitude adjustment control and the phase adjustment control of amplitude and phase adjuster 103 via leads 162 and 164 to modify its amplitude and phase characteristics, respectively. The outputs of converters 240 and 245 are sent to amplitude and phase adjuster 123 via leads 166 and 168 to modify its amplitude and phase parameters. Interface 235 is also connected to the control lead of RF switch 145 to determine its position during the control operations.

Prior to the start of operation of the circuit of FIG. 1, amplitude and phase adjusters 103 and 123 are manually trimmed to optimum settings. Controller 150 is adapted to maintain optimum operation over time under varying conditions. Amplitude and phase adjuster 103 modifies the amplitude and phase characteristics of signal s_2 so that the amplified signal component of amplifier 105 is canceled by the undistorted output signal from gain and phase adjuster 103. The controller is first connected to directional coupler 138 by RF switch 145 and directs the scanning of the frequency spectrum of the signal therefrom through VCO 152, mixer 155 and narrow band receiver 160 to detect a carrier. It is then connected to splitter 120 at the output of combiner 117 and the amplitude and phase parameters of adjuster 103 are adjusted to minimize the magnitude of the carrier appearing on lead 142. After the carrier component is minimized or a preset number of adjustments are made, the controller operates to scan the prescribed frequency band from end f_L to detect an intermodulation signal and makes a sequence of adjustments of the amplitude and phase parameters of adjuster 123 to reduce the intermodulation signal on lead 140 below a prescribed threshold. The controller continuously cycles through parameter adjustment of amplitude and phase adjusters 103 and 123.

The operation of the controller of FIG. 2 is directed by instructions permanently stored in control program store 205. FIG. 3 is a flow chart illustrating the operation of the controller 150 in accordance with the instructions stored therein. With reference to FIGS. 2 and 3, control processor 210 initially resets digital to analog converters 220, 225, 230, 240 and 245 as per program step 301. Carrier adjustment control signals and the intermodulation adjustment control signals are then initialized in steps 302 and 303 and RF switch 145 is set to receive the signal on lead 140 (step 304). At this time, VCO circuit 152 is set by digital to analog converter 220 to be at the f_L end of the prescribed frequency range of the amplifier. RF switch 145 is set to couple lead 140 to one input of mixer 145 and VCO 152 is connected to the other input of mixer 155. In the loop from step 305 to step 307, the prescribed frequency band is scanned (step 305) until a carrier signal is detected at lead 140 (step 307). Signals obtained at narrow band receiver 160 during the scan are applied to analog to digital converter 201 in FIG. 2 and stored by the control processor in data store 215. Upon detection of a carrier signal by the control processor, the carrier signal amplitude and frequency are stored and the scan frequency of VCO 152 is maintained (step 310).

Processor 210 then sends a signal to RF Switch 145 to change its position to couple the distortion signal from splitter 120 to mixer 155 (step 312). At this time, the signal on lead 142 corresponding to the detected carrier is applied from receiver 160 to analog to digital converter 201. A signal N which counts the number of carrier signal adjustments is then set to one (step 315) and the carrier signal adjustment loop from step 317 to step 330 is entered. During the iterative detected carrier signal adjustment, the parameters of amplitude and phase adjuster 103 are modified to minimize the carrier signal observed by the control processor. The loop is iterated until the carrier signal falls below a predetermined threshold or until a preset number of adjustments have been made.

In the carrier adjustment loop, the carrier signal at splitter 120 is applied to analog to digital converter 201 via RF switch 145, mixer 155 and receiver 160. The carrier magnitude data is analyzed and adjustments are made to the amplitude and phase parameters of adjuster 103 (step 317). The magnitude of the carrier signal $M(S_c)$ is compared to the predetermined threshold in decision step 320 by processor 210. Until the carrier magnitude is less than the threshold TH, the loop is iterated. If the magnitude of the carrier signal at splitter 120 is less than the threshold value, the carrier component in the output of combiner 117 in FIG. 1 is determined to be acceptable, control is passed to step 333 and the intermodulation signal reduction is started. Where the magnitude is equal to or greater than the threshold value TH, the carrier adjustment count is incremented (step 327) and compared to a predetermined number N^* (step 330). If N^* is exceeded, the iterations are terminated and

the intermodulation product signal reduction is begun in step 333. The operations of detected carrier signal data analysis step 317 are shown in greater detail in the flow chart of FIG. 4.

With reference to FIG. 4, the analysis involves separate adjustment of the amplitude and phase parameters of adjuster 103. Decision step 401 is entered from step 315 or step 330 to determine whether the amplitude or the phase parameter is to be adjusted in the current iteration. This is done by dividing the adjustment count signal N by 10. If the result is even, the control signals DR, CN and SS are set to the amplitude adjustment values DRA, CNA and SSA in step 405. Otherwise the adjustment control signals DR, CN and SS are set to DRP, CNP and SSP for phase adjustment in step 410. Assume for purposes of illustration that amplitude adjustment is selected. The direction of change control signal DR is initially set to the value, i.e., I (increase) or D (decrease), obtained in the last iteration. The condition control signal is set to either B (better) or W (worse) corresponding the corrective value of the last iteration and the correction step size SS is set to a large value, medium value or small value corresponding to the last iteration.

Decision step 415 is then entered in which the control parameters are evaluated. If $CN=B$ and $DR=I$ or $CN=W$ and $DR=D$ indicating an improvement on increase or a worsening on decrease during the last iteration, control signal DR is set to I and the control voltage on amplitude adjustment digital to analog converter 225 is increased by an amount corresponding to the setting of step size signal SS (step 425). In the event that the condition $CN=B$ and $DR=I$ or $CN=W$ and $DR=D$ is not satisfied, direction control DR is set to D and the control voltage on the amplitude adjustment converter is decreased by the amount corresponding to the last iteration step size SS (step 420). In the initial iteration, the step size is preset to zero.

After the adjustment of step 420 or step 425, the carrier detected signal amplitude $M(Sc)$ is input from receiver 160 of FIG. 1 (step 430) and compared to the amplitude of the preceding iteration $M(Sc)^*$ (step 433). If $M(Sc) \geq M(Sc)^*$, the adjustment status is worse and condition signal CN is set to W (step 438). Where $M(Sc)$ is smaller than $M(Sc)^*$, the adjustment status is better and CN is set to B (step 435). $M(Sc)^*$ is then set to the current magnitude value $M(Sc)$ in step 440 preparatory for the next iteration.

The range of the present magnitude signal $M(Sc)$ is then determined in decision steps 442, 444 and 446 so that the step size of the next iteration can be adjusted. If the magnitude of $M(Sc)$ is greater than -10 db relative to the peak of the detected carrier, the step size is set to a large value in step 450 so that the next adjustment provides a large correction. A magnitude of $M(Sc)$ between -10 and -20 db causes the step size to be set to a medium value in step 452 and a step size between -20 and -30 db generates a small step size in step 454.

If the magnitude of $M(Sc)$ is less than -30 db, the step size is set to zero in step 448. Since $N/10$ is even for amplitude adjustment, step 464 is entered via decision step 460 and the updated parameters DR, CN and SS are stored as signals DRA, CNA and SSA. If $N/10$ is odd, control parameters DR, CN and SS are stored as signals DRP, CNP and SSP in step 462. Processor control is then passed to step 320 in FIG. 3.

Where the signal $N/10$ is odd, the operation of the control processor is the same as previously described with respect to FIG. 4 except that condition control signal CNP, direction control signal DRP and step size signal SSP are obtained as indicated in step 410 and used as control signals CN, DR and SS. Maximum adjustment count signal N^* may be set to a high value so that the control processor adjusts one of the amplitude and phase parameters of adjuster 103 several times and then adjusts the other of the amplitude and phase parameters several times or until the magnitude of the carrier signal $M(Sc)$ falls below threshold TH.

When the carrier processing loop of FIG. 3 is exited via decision step 320 or 330, processor 210 causes RF switch 145 to be repositioned so that lead 140 from directional coupler 138 is connected to one input of mixer 155 and the output of receiver 160 corresponds to the output signal at lead 140 (step 333). The controller is then conditioned to scan the frequency range of the amplifier from the same end used as the starting frequency of the carrier signal to search for an intermodulation product signal (step 335). If such an intermodulation product signal is detected in step 340 prior to the carrier frequency $f(Sc)$, the intermodulation count signal M is set to one (step 343) and intermodulation adjustment loop from step 345 to step 355 is entered. Otherwise, the processor returns to step 304 so that the carrier scan process of steps 305 and 307 is restarted.

In the intermodulation reduction loop, processor 210 analyzes the intermodulation signal magnitude IM and adjusts the amplitude and phase of adjuster 123 responsive thereto (step 345). After an adjustment is made to adjuster 123, the intermodulation signal IM is tested in decision step 348. If the magnitude IM is not between -30 and -60 db, processor control is passed to step 304 and the carrier signal search loop is reentered. When the IM signal is between -30 and -60 db, another iteration of the intermodulation reduction loop is needed and intermodulation count signal M is incremented (step 352). The incremented value is compared to maximum count signal M^* (step 355) and the loop is reentered in step 345. If the magnitude IM is greater than -30 db, the detected signal may not be an intermodulation signal and control is returned to step 304. Where magnitude IM is below -60 db, the value is acceptable and step 304 is reentered. The intermodulation reduction loop may be exited from either decision steps 348 or 355.

The intermodulation signal analysis and adjustment step 345 is shown in greater detail in FIG. 5. Referring to FIG. 5, the analysis involves separate adjustment of

the amplitude and phase parameters of adjuster 123. Decision step 501 is entered from step 343 or 355 in FIG. 3 to determine whether the amplitude or the phase parameter is to be adjusted in the current iteration. This is done by dividing the adjustment count signal M by 10. If the result is even, the control signals for the adjustments DR, CN, and SS are set to previous amplitude intermodulation adjustment values DR1A, CN1A and SS1A in step 505. Otherwise, the adjustment control signals DR, CN, and SS are set to previous phase intermodulation adjustment values DR1P, CN1P and SS1P in step 510. Assume for purposes of illustration that amplitude adjustment is selected. The direction of change control signal DR is initially set to the value, i.e., I (increase) or D (decrease), obtained in the last iteration. The condition control signal is set to either B (better) or W (worse) corresponding the corrective value of the last iteration and the correction step size SS is set to a large value, medium value or small value corresponding to the last iteration.

Decision step 515 is then entered wherein the control parameters are evaluated. If $CN=B$ and $DR=I$ or $CN=W$ and $DR=D$, indicating an improvement on increase or a worsening on decrease during the last iteration, control signal DR is set to I and the control voltage on amplitude adjustment digital to analog converter 240 is increased by an amount corresponding to the setting of step size signal SS (step 525). In the event that the condition $CN=B$ and $DR=I$ or $CN=W$ and $DR=D$ is not satisfied, direction control DR is set to D and the control voltage on the amplitude adjustment converter is decreased by the amount corresponding to the last iteration step size SS (step 520). In the initial iteration, the step size is preset to zero.

After the adjustment of step 520 or step 525, the intermodulation signal amplitude IM is input from receiver 160 of FIG. 1 (step 530) and compared to the amplitude of the preceding iteration IM^* (step 533). If $IM \geq IM^*$, the adjustment status is worse and condition signal CN is set to W (step 538). Where IM is smaller than IM^* , the adjustment status is better and CN is set to B (step 535). IM^* is then set to the current magnitude value IM in step 540 preparatory for the next iteration.

The range of the present magnitude signal IM is then determined in decision steps 542, 544 and 546 so that the step size of the next iteration can be adjusted. If the magnitude of IM is greater than -40 db relative to the peak of the detected carrier the step size is set to a large value in step 550 and the next adjustment provides a large correction. A magnitude of IM between -40 and -50 db causes the step size to be set to a medium value in step 552 and a step size between -50 and -60 db generates a small step size in step 554. If the magnitude of IM is less than -60 db, the step size is set to zero in step 548. Since $M/10$ is even for amplitude adjustment, step 564 is entered via decision step 560 and the updated parameters DR, CN and SS stored as signals DR1A, CN1A and SS1A. If $M/10$ is odd, control parameters DR,

CN and SS are stored as signals DR1P, CN1P and SS1P in step 562. Processor control is then passed to step 348 in FIG. 3.

Where the signal $M/10$ is odd (phase adjustment), the operation of the control processor is the same as previously described with respect to FIG. 5 except that condition control signal CN1P, direction control signal DR1P and step size signal SS1P are obtained as indicated in step 510 and used as control signals CN, DR and SS. Maximum adjustment count signal M^* may be set to a high value so that the control processor adjusts one of the amplitude and phase parameters of adjuster 103 several times and then adjusts the other of the amplitude and phase parameters several times or until the condition of step 448 is met.

When the data analysis and comparison of steps 345 and 348 are completed, intermodulation count M is incremented (step 352) and the count is compared to the maximum allowable count $M(Sc)^*$ in decision step 355. If $M > M^*$, step 304 is reentered to begin the carrier signal search operations. Where $M \leq M^*$ in step 355, the next iteration is then started in step 345. The iterations are ended when the intermodulation product signal is outside the -30 to -60 db range set in decision step 348 or the iterations time out in step 355 because count signal $M > M^*$. As a result of the intermodulation reduction loop operation, the intermodulation distortion is reduced by readjusting the parameters of amplitude and phase adjuster 123 until an acceptable level of intermodulation distortion is obtained.

FIG. 6 depicts a block diagram of another embodiment illustrative of the invention in which the prescribed frequency range of the amplifier circuit is scanned preferably from the center of the band f_c to the high end to locate a frequency at which there is no carrier or other signal except noise. Upon detection of a location in the frequency range where only noise is detected, a pilot signal having the detected frequency is introduced into the input of the power amplifier. The pilot operates in the same manner as the detected carrier signal described with respect to FIG. 1 so that the parameters of the amplitude and phase adjuster for the elimination of the carrier signal may be modified to minimize the pilot signal and the parameters of the gain and phase adjuster to modify the distortion signal may be changed to minimize the intermodulation products signal.

Referring to FIG. 6, the first circuit path includes splitter 601, predistortion amplifier 605 and directional coupler 610 which operate as described with respect to FIG. 1. In addition, directional coupler 676 is inserted before splitter 601 so that a pilot signal may be introduced. The second circuit path comprises gain and phase adjuster 603, delay 604 and combiner 617. Combiner 617 cancels the amplified signal component from predistortion amplifier 605 with the input signal from the gain and phase adjustment circuit path so that the distortion component appears at the input of splitter 620. Amplitude and phase adjuster 623 modifies the distor-

tion component from combiner 617 and applies the modified distortion component to combiner 615 via voltage amplifier 627 so that the phase inverted prescribed distortion is applied to the inputs of paralleled amplifiers 635-1 through 635-N. The amplifier output is obtained at lead 680 via directional coupler 638. In FIG. 6, the pilot signal is introduced into both the predistortion amplifier path and the gain and phase adjustment path and the magnitude of the pilot signal at the output of combiner 617 is used to adjust the amplitude and phase parameters of adjuster 603 to keep the pilot signal magnitude at the combiner output at its minimum value.

Controller 650 is substantially the same as controller 150 of FIG. 1 except that the instructions in control program store 205 are modified to scan the prescribed frequency band from end f_c to locate a frequency at which there is no signal and to insert a pilot signal at that frequency into directional coupler 676. In order to generate a pilot signal, VCO 652 drives frequency shifter 670 so that it produces a signal at the detected frequency. The inserted pilot then operates as a carrier as described with respect to the flow charts of FIGS. 3 and 4. The operations of FIG. 3 and FIG. 5 with respect to intermodulation product signal reduction are unchanged. Thus rather than scanning for a carrier signal as in steps 305 and 307, the scan steps illustrated in FIG. 7 are performed.

With reference to FIG. 7, digital to analog converters 225, 230, 240 and 245 are initially reset in step 701 and the pilot adjust and intermodulation adjust control signals are initialized in steps 702 and 703. RF switch 645 is then set to couple the signal on lead 640 to mixer 655 (step 704) and controller 650 is directed to scan from one end of the prescribed frequency band for a frequency at which there is no signal (step 705). When the absence of a signal is detected in step 707, the detected frequency is stored (step 710) in data store 215 of FIG. 2. RF switch 645 is then set to connect splitter 620 to mixer 655 (step 712) and the pilot adjust count signal in the controller processor is reset to one (step 714). A pilot signal is then turned on in VCO 652 and converted to the detected frequency in frequency shifter 670. The detected frequency pilot signal is then applied to directional coupler 676 (step 715). The remaining operations of FIG. 7 correspond to the operations with respect to FIG. 1 shown in FIG. 3 except that the magnitude of the pilot signal is analyzed in step 717 of FIG. 7 and FIG. 4 and the pilot signal is turned off after the pilot minimizing operations are completed (step 723 of FIG. 7). The intermodulation signal reduction in steps 733 through 755 are the same as the corresponding steps in FIG. 3 and FIG. 5 and the intermodulation signal is the first such signal detected in the scan operations of steps 735 and 740. Advantageously, the pilot is inserted at any unused part of the amplifier frequency band and the full frequency band except for the unused pilot frequency may be used for transmission.

Claims

1. A distortion compensation circuit comprising:

a power amplifier (135-N) having a prescribed distortion characteristic; means (101) for receiving one or more input signals including at least one carrier signal in a predetermined frequency range;

a first circuit path having an input connected to the receiving means, an output, and a first amplifier (105) with a predetermined gain and substantially the same prescribed distortion characteristic as the power amplifier, the first amplifier being connected to be responsive to the one or more input signals for generating an output signal including a component corresponding to the one or more input signals modified by said predetermined gain and a distortion component corresponding to the prescribed distortion characteristic;

a second circuit path having an input connected to the receiving means and an output for transferring the one or more input signals without distortion;

first means (117) for combining the output of the first circuit path with the transferred one or more signals from the output of the second circuit path to form a signal corresponding to the distortion component of the first circuit path output signal;

second means (115) for combining the distortion component signal from the first combining means with the output signal of the first circuit path to form a signal having a component corresponding to the one or more input signals modified by the predetermined gain and a component corresponding to the distortion characteristic of the first amplifier in inverted phase relationship thereto; and

means for controlling the signal formed in the first combining means;

CHARACTERIZED IN THAT

the controlling means comprises

means (140,150,160) for detecting a carrier signal in the predetermined frequency range;

means (142,150,160) connected to the output of the first combining means for monitoring the detected carrier signal at the output of the first combining means; and

means (103) in the second circuit path responsive to the output of said monitoring means for adjusting the magnitude and phase of the signal applied to the second circuit path to minimize the monitored carrier signal.

2. A circuit according to claim 1 wherein said detecting means (140,150,160) comprises means (150,152,

- 155) connected to the output of said power amplifier for scanning the predetermined frequency range for a signal at said power amplifier output having a magnitude above a first predetermined threshold.
3. A circuit according to claim 2 wherein said monitoring means (142,150,160) comprises
- means (155,160) for generating a signal representative of the magnitude of the detected carrier signal;
 - means (150,317) connected between the generating means and the adjusting means and responsive to the signal representative of the magnitude of the detected carrier signal for producing first and second adjusting signals;
 - means (162) for applying the first adjusting signal to modify the magnitude of the signal applied to the second circuit path; and
 - means (164) for applying the second adjusting signal to modify the phase of the signal applied to the second circuit path.
4. A circuit according to claim 3 wherein the means (150,317) for producing said first and second adjusting signal comprises means (150,450,452,454) responsive to the magnitude of the detected carrier signal for sequentially producing one or more first adjusting signals until a fixed number of first adjusting signals is reached or the magnitude of the monitored detected carrier signal falls below the first threshold, and for sequentially producing one or more second adjusting signals until a fixed number of second adjusting signals is reached or the magnitude of the monitored detected carrier signal falls below the first threshold.
5. A circuit according to claim 4 wherein the scanning means (150,152,155) comprises
- means (152,155) responsive to the output of the power amplifier for changing the frequency of the signals from the output of the power amplifier to a predetermined frequency; and
 - a narrow band receiver (160) for receiving the scanned signals at the predetermined frequency.
6. A circuit according to claim 1 wherein the power amplifier (135-N) comprises a plurality of amplifiers (135-1 - 135-N) connected in parallel, each amplifier (e. g. 135-1) having the prescribed distortion characteristic, and the first amplifier (105) has substantially the same distortion characteristic as each of the plurality of amplifiers connected in parallel.
7. A circuit according to claim 1 comprising means (140,142,150,160) for controlling the signal formed
- in said second combining means, comprising
- means (140,150,152,155,160) connected to the output of the power amplifier for detecting an intermodulation product signal in the predetermined frequency range and for monitoring the detected intermodulation product signal at the output of the power amplifier; and
 - means (123,127) connected between the first and second combining means for adjusting the magnitude and phase of the first combining means output signal to minimize the monitored intermodulation product signal.
8. A circuit according to claim 7 wherein the means (123,127) for adjusting the magnitude and phase of the first combining means output signal comprises means (127) for inverting the phase of the first combining means output signal.
9. A circuit according to claim 8 wherein said means (140,150,152,155,160) for detecting an intermodulation product signal comprises means (140,150,152,155) connected to the output of said power amplifier for scanning the predetermined frequency range for a signal at said power amplifier output having a magnitude between a first predetermined threshold and a second predetermined threshold below the first threshold.
10. A circuit according to claim 9 wherein said means (140,150,152,155,160) for monitoring said detected intermodulation product signal comprises
- means (160) for generating a signal representative of the magnitude of the detected intermodulation product signal;
 - means (150,348) connected to the generating means for producing first and second adjusting signals;
 - means (166) for applying the first adjusting signal to the means for adjusting the magnitude and phase of the first combining means output signal to modify the magnitude of the first combining means output signal; and
 - means (168) for applying the second adjusting signal to the means for adjusting the magnitude and phase of the first combining means output signal to modify the phase of the first combining means output signal.
11. A circuit according to claim 10 wherein the means (150,348) for producing said first and second adjusting signals comprises means (150,345,348,352,355) responsive to the magnitude of the monitored intermodulation product signal for sequentially producing one or more first adjusting signals until a fixed number of first adjusting signals is reached

or the magnitude of the monitored intermodulation product signal falls below the second threshold, and for sequentially producing one or more second adjusting signals until a fixed number of second adjusting signals is reached or the magnitude of the monitored intermodulation product signal falls below the second threshold.

12. A circuit according to claim 11 wherein the scanning means (150, 152, 155) comprises

means (140, 152, 155) responsive to the output of the power amplifier for changing the frequency of the signals from the output of the power amplifier to a predetermined frequency; and a narrow band receiver (160) for receiving the predetermined frequency.

13. A circuit according to claim 7 wherein the power amplifier comprises a plurality of amplifiers (135-1 - 135-N) connected in parallel, each amplifier (e.g. 135-1) having the prescribed distortion characteristic, and the first amplifier (105) has substantially the same distortion characteristic as each of the plurality of amplifiers connected in parallel.

14. A circuit according to claim 1 wherein the detecting means (140, 150, 160) comprises

means (640, 650, 660) for detecting a frequency in the predetermined frequency range at which said one or more input signals are absent; means (640, 650, 652, 670) for generating a pilot signal at said detected frequency and for applying said pilot signal to the receiving means; and means (642, 650, 655, 660) connected to the output of the first combining means for monitoring the pilot signal at the output of the first combining means.

15. A circuit according to claim 14 wherein said means (640, 650, 660) for detecting the frequency in the predetermined frequency range at which said one or more input signals are absent comprises means (640, 650, 652, 655) connected to the output of said power amplifier for scanning the predetermined frequency range for a signal at said power amplifier output having a magnitude less than a first predetermined threshold.

16. A circuit according to claim 15 wherein said means (640, 650, 655, 660) for monitoring the pilot signal comprises

means (650, 660) for generating a signal representative of the magnitude of the pilot signal; means (650, 717) connected between the means for generating a signal representative of

the magnitude of the pilot signal and the adjusting means (603) and responsive to the signal representative of the magnitude of the pilot signal for producing first and second adjusting signals;

means (662) for applying the first adjusting signal to modify the magnitude of the signal applied to the second circuit path; and

means (664) for applying the second adjusting signal to modify the phase of the signal applied to the second circuit path.

Patentansprüche

1. Verzerrungskompensationsschaltung mit folgenden:

einem Leistungsverstärker (135-N) mit einer vorgeschriebenen Verzerrungskennlinie; Mitteln (101) zum Empfangen eines oder mehrerer Eingangssignale mit mindestens einem Trägersignal in einem vorbestimmten Frequenzbereich;

einem ersten Schaltungsweg, bei dem ein Eingang mit den Empfangsmitteln verbunden ist, mit einem Ausgang und einem ersten Verstärker (105) mit einer vorbestimmten Verstärkung und im wesentlichen derselben vorgeschriebenen Verzerrungskennlinie wie der Leistungsverstärker, wobei der erste Verstärker so geschaltet ist, daß er auf das eine oder mehrere Eingangssignale reagiert, um ein Ausgangssignal mit einer dem einen oder mehreren Eingangssignalen, verändert durch die besagte vorbestimmte Verstärkung, entsprechenden Komponente und einer der vorgeschriebenen Verzerrungskennlinie entsprechenden Verzerrungskomponente zu erzeugen;

einem zweiten Schaltungsweg, bei dem ein Eingang mit den Empfangsmitteln verbunden ist, und mit einem Ausgang zur Übertragung des einen oder mehrerer Eingangssignale ohne Verzerrung;

ersten Mitteln (117) zum Kombinieren des Ausgangssignals des ersten Schaltungsweges mit dem übertragenen einen oder mehreren Signalen vom Ausgang des zweiten Schaltungsweges, um ein der Verzerrungskomponente des Ausgangssignals des ersten Schaltungsweges entsprechendes Signal zu bilden;

zweiten Mitteln (115) zum Kombinieren des Verzerrungskomponentensignals von den ersten Kombiniermitteln mit dem Ausgangssignal des ersten Schaltungsweges, um ein Signal zu bilden, das eine dem einen oder mehreren Eingangssignalen, verändert durch die vorbestimmte Verstärkung, entsprechende Kompo-

- nente und eine der Verzerrungskennlinie des ersten Verstärkers im umgekehrten Phasenverhältnis dazu entsprechende Komponente aufweist; und
Mitteln zum Steuern des in den ersten Kombiniernmitteln gebildeten Signals; dadurch gekennzeichnet, daß die Steuermittel folgendes umfassen:
Mittel (140, 150, 160) zum Erkennen eines Trägersignals im vorbestimmten Frequenzbereich;
mit dem Ausgang der ersten Kombiniernmittel verbundene Mittel (142, 150, 160) zum Überwachen des erkannten Trägersignals am Ausgang der ersten Kombiniernmittel; und
auf das Ausgangssignal der besagten Überwachungsmittel reagierende Mittel (103) dem zweiten Schaltungsweg zum Einstellen der Größe und Phase des an den zweiten Schaltungsweg angelegten Signals zur Minimierung des überwachten Trägersignals.
2. Schaltung nach Anspruch 1, wobei die besagten Erkennungsmittel (140, 150, 160) mit dem Ausgang des besagten Leistungsverstärkers verbundene Mittel (150, 152, 155) zum Abtasten des vorbestimmten Frequenzbereichs auf ein Signal am besagten Leistungsverstärkerausgang mit einer ersten vorbestimmten Schwellwert überschreitenden Größe umfassen.
3. Schaltung nach Anspruch 2, wobei die besagten Überwachungsmittel (142, 150, 160) folgendes umfassen:
Mittel (155, 160) zum Erzeugen eines die Größe des Trägersignals darstellenden Signals; zwischen die besagten Erzeugungsmittel und die Einstellmittel geschaltete Mittel (150, 317), die auf das die Größe des erkannten Trägersignals darstellende Signal reagieren, um erste und zweite Einstellsignale zu erzeugen; Mittel (162) zum Anlegen des ersten Einstellsignals zur Veränderung der Größe des an den zweiten Schaltungsweg angelegten Signals; und
Mittel (164) zum Anlegen des zweiten Einstellsignals zur Veränderung der Phase des an den zweiten Schaltungsweg angelegten Signals.
4. Schaltung nach Anspruch 3, wobei die Mittel (150, 317) zum Erzeugen des besagten ersten und zweiten Einstellsignals Mittel (150, 450, 452, 454) umfassen, die auf die Größe des erkannten Trägersignals reagieren, um sequentiell ein oder mehrere erste Einstellsignale zu erzeugen, bis eine feste Anzahl erster Einstellsignale erreicht ist oder die Größe des überwachten erkannten Trägersignals den ersten Schwellwert unterschreitet, und um sequentiell ein oder mehrere zweite Einstellsignale zu erzeugen, bis eine feste Anzahl zweiter Einstellsignale erreicht ist oder die Größe des überwachten erkannten Trägersignals den ersten Schwellwert unterschreitet.
5. Schaltung nach Anspruch 4, wobei die Abtastmittel (150, 152, 155) folgendes umfassen:
auf das Ausgangssignal des Leistungsverstärkers reagierende Mittel (152, 155) zum Verändern der Frequenz der Signale vom Ausgang des Leistungsverstärkers auf eine vorbestimmte Frequenz; und
einen Schmalbandempfänger (160) zum Empfangen der abgetasteten Signale mit der vorbestimmten Frequenz.
6. Schaltung nach Anspruch 1, wobei der Leistungsverstärker (135-N) eine Mehrzahl von parallel geschalteten Verstärkern (135-1 - 135-N) umfaßt, wobei jeder Verstärker (z.B. 135-1) die vorgeschriebene Verzerrungskennlinie aufweist und der erste Verstärker (105) im wesentlichen dieselbe Verzerrungskennlinie wie jeder der Mehrzahl von parallel geschalteten Verstärkern aufweist.
7. Schaltung nach Anspruch 1 mit Mitteln (140, 142, 150, 160) zum Steuern des in den besagten zweiten Kombiniernmitteln gebildeten Signals mit folgenden:
mit dem Ausgang des Leistungsverstärkers verbundenen Mitteln (140, 150, 152, 155, 160) zum Erkennen eines Intermodulationsproduktsignals im vorbestimmten Frequenzbereich und zum Überwachen des erkannten Intermodulationsproduktsignals am Ausgang des Leistungsverstärkers; und
zwischen die ersten und zweiten Kombiniernmittel geschaltete Mittel (123, 127) zum Einstellen der Größe und Phase des Ausgangssignals der ersten Kombiniernmittel zum Minimieren des überwachten Intermodulationsproduktsignals.
8. Schaltung nach Anspruch 7, wobei die Mittel (123, 127) zum Einstellen der Größe und Phase des Ausgangssignals der ersten Kombiniernmittel Mittel (127) zum Invertieren der Phase des Ausgangssignals der ersten Kombiniernmittel umfassen.
9. Schaltung nach Anspruch 8, wobei die besagten Mittel (140, 150, 152, 155, 160) zum Erkennen eines Intermodulationsproduktsignals mit dem Ausgang des besagten Leistungsverstärkers verbundene Mittel (140, 150, 152, 155) zum Abtasten des vorbestimmten Frequenzbereichs auf ein Signal am besagten Leistungsverstärkerausgang mit einer

Größe zwischen einem ersten vorbestimmten Schwellwert und einem zweiten vorbestimmten Schwellwert unterhalb des ersten Schwellwerts umfassen:

10. Schaltung nach Anspruch 9, wobei die besagten Mittel (140, 150, 152, 155, 160) zum Überwachen des besagten erkannten Intermodulationsproduktsignals folgendes umfassen:

Mittel (160) zum Erzeugen eines die Größe des erkannten Intermodulationsproduktsignals darstellenden Signals;

mit den Erzeugungsmitteln verbundene Mittel (150, 348) zum Erzeugen erster und zweiter Einstellsignale;

Mittel (166) zum Anlegen des ersten Einstellsignals an die Mittel zum Einstellen der Größe und Phase des Ausgangssignals der ersten Kombiniermittel zum Verändern der Größe des Ausgangssignals der ersten Kombiniermittel; und

Mittel (168) zum Anlegen des zweiten Einstellsignals an die Mittel zum Einstellen der Größe und Phase des Ausgangssignals der ersten Kombiniermittel zum Verändern der Phase des Ausgangssignals der ersten Kombiniermittel.

11. Schaltung nach Anspruch 10, wobei die Mittel (150, 348) zum Erzeugen der besagten ersten und zweiten Einstellsignale Mittel (150, 345, 348, 352, 355) umfassen, die auf die Größe des überwachten Intermodulationsproduktsignals reagieren, um sequentiell ein oder mehrere erste Einstellsignale zu erzeugen, bis eine feste Anzahl erster Einstellsignale erreicht ist oder die Größe des überwachten Intermodulationsproduktsignals den zweiten Schwellwert unterschreitet, und um sequentiell ein oder mehrere zweite Einstellsignale zu erzeugen, bis eine feste Anzahl zweiter Einstellsignale erreicht ist oder die Größe des überwachten Intermodulationsproduktsignals den zweiten Schwellwert unterschreitet.

12. Schaltung nach Anspruch 11, wobei die Abtastmittel (150, 152, 155) folgendes umfassen:

auf das Ausgangssignal des Leistungsverstärkers reagierende Mittel (140, 152, 155) zum Ändern der Frequenz der Signale vom Ausgang des Leistungsverstärkers auf eine vorbestimmte Frequenz; und
einen Schmalbandempfänger (160) zum Empfangen der vorbestimmten Frequenz.

13. Schaltung nach Anspruch 7, wobei der Leistungsverstärker eine Mehrzahl von parallel geschalteten Verstärkern (135-1 - 135-N) umfaßt, wobei jeder

Verstärker (z.B. 135-1) die vorgeschriebene Verzerrungskennlinie aufweist und der erste Verstärker (105) im wesentlichen dieselbe Verzerrungskennlinie wie jeder der Mehrzahl von parallel geschalteten Verstärkern aufweist.

14. Schaltung nach Anspruch 1, wobei die Erkennungsmittel (140, 150, 160) folgendes umfassen:

Mittel (640, 650, 660) zum Erkennen einer Frequenz im vorbestimmten Frequenzbereich, bei der besagtes eines oder mehrere Eingangssignale abwesend sind;

Mittel (640, 650, 652, 670) zum Erzeugen eines Pilotsignals mit der besagten erkannten Frequenz und zum Anlegen des besagten Pilotsignals an die Empfangsmittel; und

mit dem Ausgang der ersten Kombiniermittel verbundene Mittel (642, 650, 655, 660) zum Überwachen des Pilotsignals am Ausgang der ersten Kombiniermittel.

15. Schaltung nach Anspruch 14, wobei die besagten Mittel (640, 650, 660) zum Erkennen der Frequenz im vorbestimmten Frequenzbereich, bei der das besagte eine oder mehrere Eingangssignale abwesend sind, mit dem Ausgang des besagten ersten Verstärkers verbundene Mittel (640, 650, 652, 655) zum Abtasten des vorbestimmten Frequenzbereichs auf ein Signal am besagten Leistungsverstärkerausgang mit einer geringeren Größe als ein erster vorbestimmter Schwellwert umfassen.

16. Schaltung nach Anspruch 15, wobei besagte Mittel (640, 650, 655, 660) zum Überwachen des Pilotsignals folgendes umfassen:

Mittel (650, 660) zum Erzeugen eines die Größe des Pilotsignals darstellenden Signals;

zwischen die Mittel zum Erzeugen eines die Größe des Pilotsignals darstellenden Signals und die Einstellmittel (603) geschaltete und auf die Größe des Pilotsignals reagierende Mittel (650, 717) zum Erzeugen erster und zweiter Einstellsignale;

Mittel (662) zum Anlegen des ersten Einstellsignals zur Veränderung der Größe des an den zweiten Schaltungsweg angelegten Signals; und

Mittel (664) zum Anlegen des zweiten Einstellsignals zur Veränderung der Phase des an den zweiten Schaltungsweg angelegten Signals.

55 Revendications

1. Circuit de compensation de distorsion comprenant:

un amplificateur linéaire (135-N) ayant une caractéristique de distorsion prescrite;

un moyen (101) pour recevoir un ou plusieurs signaux d'entrée comportant au moins un signal de porteuse dans une gamme de fréquences prédéterminée;

un premier chemin de circuit ayant une entrée connectée au moyen de réception, une sortie, et un premier amplificateur (105) ayant un gain prédéterminé et substantiellement la même caractéristique de distorsion prescrite que l'amplificateur linéaire, le premier amplificateur étant connecté pour être sensible au ou aux plusieurs signaux d'entrée pour générer un signal de sortie comportant une composante correspondant au ou aux plusieurs signaux modifiés par ledit gain prédéterminé et une composante de distorsion correspondant à la caractéristique de distorsion prescrite;

un deuxième chemin de circuit ayant une entrée connectée au moyen de réception et une sortie pour transférer le ou les signaux d'entrée sans distorsion;

un premier moyen (117) pour combiner la sortie du premier chemin de circuit avec le ou les plusieurs signaux transférés à partir de la sortie du deuxième chemin de circuit pour former un signal correspondant à la composante de distorsion du signal de sortie du premier chemin de circuit;

un deuxième moyen (115) pour combiner le signal de composante de distorsion provenant du premier moyen de combinaison avec le signal de sortie du premier chemin de circuit pour former un signal ayant une composante correspondant au ou aux plusieurs signaux d'entrée modifiés par le gain prédéterminé et une composante correspondant à la caractéristique de distorsion du premier amplificateur en relation de phase inversée avec elle; et

un moyen pour commander le signal formé dans le premier moyen de combinaison;

CHARACTERISE EN CE QUE

le moyen de commande comprend un moyen (140,150,160) pour détecter un signal de porteuse dans la gamme de fréquences prédéterminée;

un moyen (142,150,160) connecté à la sortie du premier moyen de combinaison pour contrôler le signal de porteuse détecté à la sortie du premier moyen de combinaison; et

un moyen (103) dans le deuxième chemin de circuit sensible à la sortie dudit moyen de contrôle pour régler l'amplitude et la phase du signal appliqué au deuxième chemin de circuit pour minimiser le signal de porteuse contrôlé.

2. Circuit selon la revendication 1, dans lequel ledit

moyen de détection (140,150,160) comprend un moyen (150,152,155) connecté à la sortie dudit amplificateur de puissance pour balayer la gamme de fréquences prédéterminée à la recherche d'un signal à la sortie dudit amplificateur de puissance ayant une amplitude au-dessus d'un premier seuil prédéterminé.

3. Circuit selon la revendication 2, dans lequel ledit moyen de contrôle (142,150,160) comprend

un moyen (155,160) pour générer un signal représentatif de l'amplitude du signal de porteuse détecté;

un moyen (150,317) connecté entre le moyen de génération et le moyen de réglage et sensible au signal représentatif de l'amplitude du signal de porteuse détecté pour produire des premier et deuxième signaux de réglage;

un moyen (162) pour appliquer le premier signal de réglage pour modifier l'amplitude du signal appliqué au deuxième chemin de circuit; et un moyen (164) pour appliquer le deuxième signal de réglage pour modifier la phase du signal appliqué au deuxième chemin de circuit.

4. Circuit selon la revendication 3, dans lequel le moyen (150,317) pour produire lesdits premier et deuxième signaux de réglage comprend un moyen (150,450,452,454) sensible à l'amplitude du signal de porteuse détecté pour produire séquentiellement un ou plusieurs premiers signaux de réglage jusqu'à ce qu'un nombre fixe de premiers signaux de réglage soit atteint ou que l'amplitude du signal de porteuse détecté contrôlé chute en dessous du premier seuil, et pour produire séquentiellement un ou plusieurs deuxièmes signaux de réglage jusqu'à ce qu'un nombre fixe de deuxièmes signaux de réglage soit atteint ou que l'amplitude du signal de porteuse détecté contrôlé chute en dessous du premier seuil.

5. Circuit selon la revendication 4, dans lequel le moyen de balayage (150,152,155) comprend

un moyen (152,155) sensible à la sortie de l'amplificateur de puissance pour changer la fréquence des signaux provenant de la sortie de l'amplificateur de puissance à une fréquence prédéterminée; et

un récepteur à bande étroite (160) pour recevoir les signaux balayés à la fréquence prédéterminée.

6. Circuit selon la revendication 1, dans lequel l'amplificateur de puissance (135-N) comprend une pluralité d'amplificateurs (135-1 à 135-N) connectés en parallèle, chaque amplificateur (p. ex. 135-1) ayant

la caractéristique de distorsion prescrite, et le premier amplificateur (105) a substantiellement la même caractéristique de distorsion que chacun de la pluralité des amplificateurs connectés en parallèle.

7. Circuit selon la revendication 1, comprenant un moyen (140,142,150,160) pour commander le signal formé dans ledit deuxième moyen de combinaison, comprenant

un moyen (140,150,152,155,160) connecté à la sortie de l'amplificateur de puissance pour détecter un signal de produit d'intermodulation dans la gamme de fréquences prédéterminée et pour contrôler le signal de produit d'intermodulation détecté à la sortie de l'amplificateur de puissance; et
un moyen (123,127) connecté entre les premier et deuxième moyens de combinaison pour régler l'amplitude et la phase du signal de sortie du premier moyen de combinaison pour minimiser le signal de produit d'intermodulation contrôlé.

8. Circuit conformément à la revendication 7, dans lequel le moyen (123,127) pour régler l'amplitude et la phase du signal de sortie du premier moyen de combinaison comprend un moyen (127) pour inverser la phase du signal de sortie du premier moyen de combinaison.

9. Circuit selon la revendication 8, dans lequel ledit moyen (140,150,152,155,160) pour détecter un signal de produit d'intermodulation comprend un moyen (140,150,152,155) connecté à la sortie dudit amplificateur de puissance pour balayer la gamme de fréquences prédéterminée à la recherche d'un signal à la sortie dudit amplificateur de puissance ayant une amplitude entre un premier seuil prédéterminé et un deuxième seuil prédéterminé en dessous du premier seuil.

10. Circuit selon la revendication 9, dans lequel ledit moyen (140,150,152,155,160) pour contrôler ledit signal de produit d'intermodulation comprend

un moyen (160) pour générer un signal représentatif de l'amplitude du signal d'intermodulation détecté;
un moyen (150,348) connecté au moyen de génération pour produire des premier et deuxième signaux de réglage;
un moyen (166) pour appliquer le premier signal de réglage au moyen de réglage de l'amplitude et de la phase du signal de sortie du premier moyen de combinaison pour modifier l'amplitude du signal de sortie du premier moyen de combinaison; et

un moyen (168) pour appliquer le deuxième signal de réglage au moyen de réglage de l'amplitude et de la phase du signal de sortie du premier moyen de combinaison pour modifier la phase du signal de sortie du premier moyen de combinaison.

11. Circuit selon la revendication 10, dans lequel le moyen (150,348) pour produire lesdits premier et deuxième signaux de réglage comprend un moyen (150,345,348,352,355) sensible à l'amplitude du signal de produit d'intermodulation contrôlé pour produire séquentiellement un ou plusieurs premiers signaux de réglage jusqu'à ce qu'un nombre fixe de premiers signaux de réglage soit atteint ou que l'amplitude du signal de produit d'intermodulation contrôlé chute en dessous du deuxième seuil, et pour produire séquentiellement un ou plusieurs deuxièmes signaux de réglage jusqu'à ce qu'un nombre fixe de deuxièmes signaux de réglage soit atteint ou que l'amplitude du signal de produit d'intermodulation contrôlé chute en dessous du deuxième seuil.

12. Circuit selon la revendication 11, dans lequel le moyen de balayage (150,152,155) comprend

un moyen (140,152,155) sensible à la sortie de l'amplificateur de puissance pour changer la fréquence des signaux provenant de la sortie de l'amplificateur de puissance à une fréquence prédéterminée; et
un récepteur à bande étroite (160) pour recevoir la fréquence prédéterminée.

13. Circuit selon la revendication 7, dans lequel l'amplificateur de puissance comprend une pluralité d'amplificateurs (135-1 à 135-N) connectés en parallèle, chaque amplificateur (p. ex. 135-1) ayant la caractéristique de distorsion prescrite, et le premier amplificateur (105) a substantiellement la même caractéristique de distorsion que chacun de la pluralité des amplificateurs connectés en parallèle.

14. Circuit selon la revendication 1, dans lequel le moyen de détection (140,150,160) comprend

un moyen (640,650,660) pour détecter une fréquence dans la gamme de fréquences prédéterminée à laquelle lesdits un ou plusieurs signaux d'entrée sont absents;
un moyen (640,650,652,670) pour générer un signal pilote à ladite fréquence détectée et pour appliquer ledit signal pilote au moyen de réception; et
un moyen (642,650,655,660) connecté à la sortie du premier moyen de combinaison pour contrôler le signal pilote à la sortie du premier

moyen de combinaison.

15. Circuit selon la revendication 14, dans lequel ledit moyen (640,650,660) pour détecter la fréquence dans la gamme de fréquences prédéterminée à laquelle lesdits un ou plusieurs signaux d'entrée sont absents comprend un moyen (640,650,652,655) connecté à la sortie dudit amplificateur de puissance pour balayer la gamme de fréquences prédéterminée à la recherche d'un signal à la sortie dudit amplificateur de puissance ayant une amplitude inférieure à un premier seuil prédéterminé.

16. Circuit selon la revendication 15, dans lequel ledit moyen (640,650,655,660) pour contrôler le signal pilote comprend.

un moyen (650,660) pour générer un signal représentatif de l'amplitude du signal pilote;
un moyen (650,717) connecté entre le moyen de génération d'un signal représentatif de l'amplitude du signal pilote et le moyen de réglage (603) et sensible au signal représentatif de l'amplitude du signal pilote pour produire des premier et deuxième signaux de réglage;
un moyen (662) pour appliquer le premier signal de réglage pour modifier l'amplitude du signal appliqué au deuxième chemin de circuit; et
un moyen (664) pour appliquer le deuxième signal de réglage pour modifier la phase du signal appliqué au deuxième chemin de circuit.

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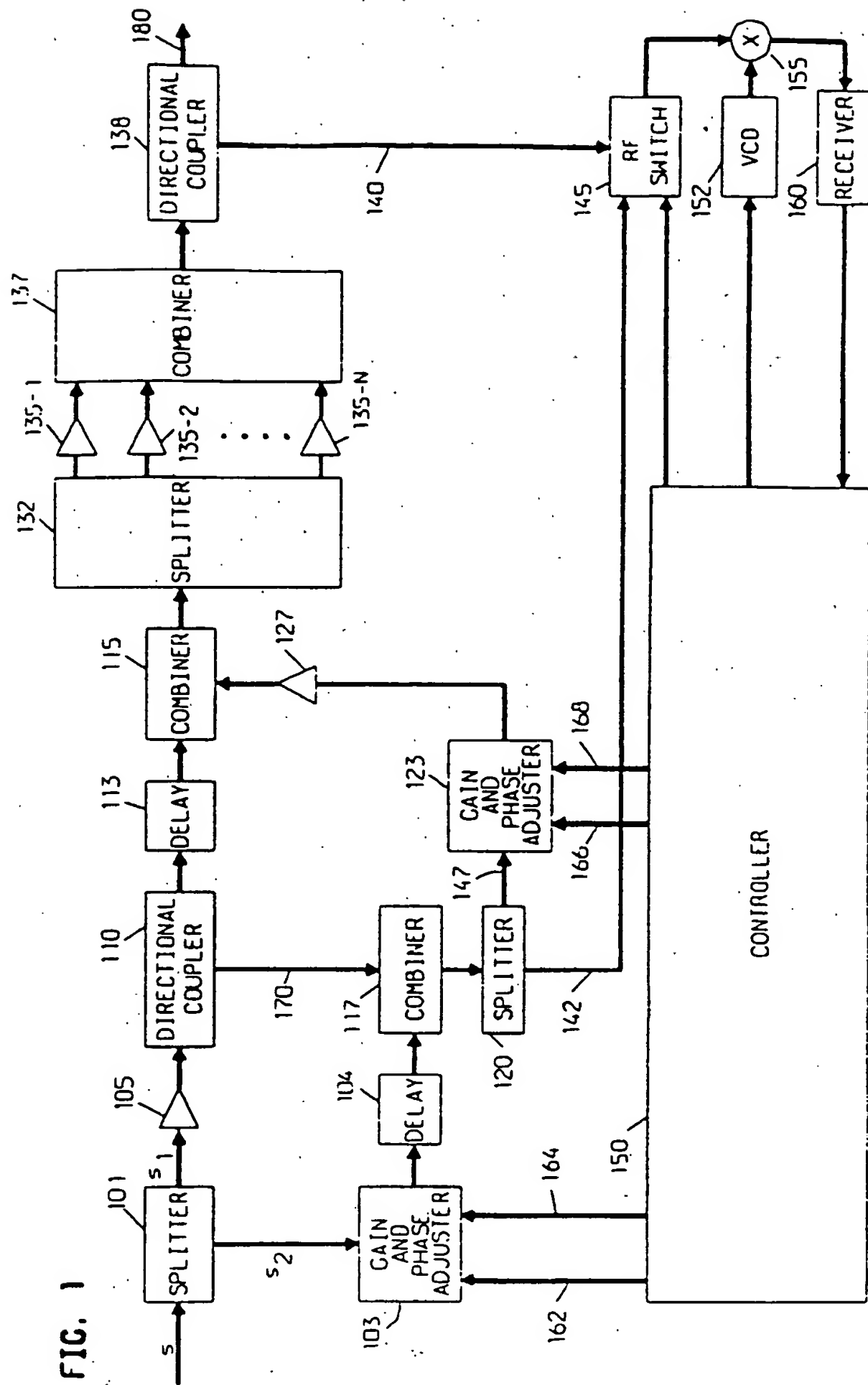


FIG. 2

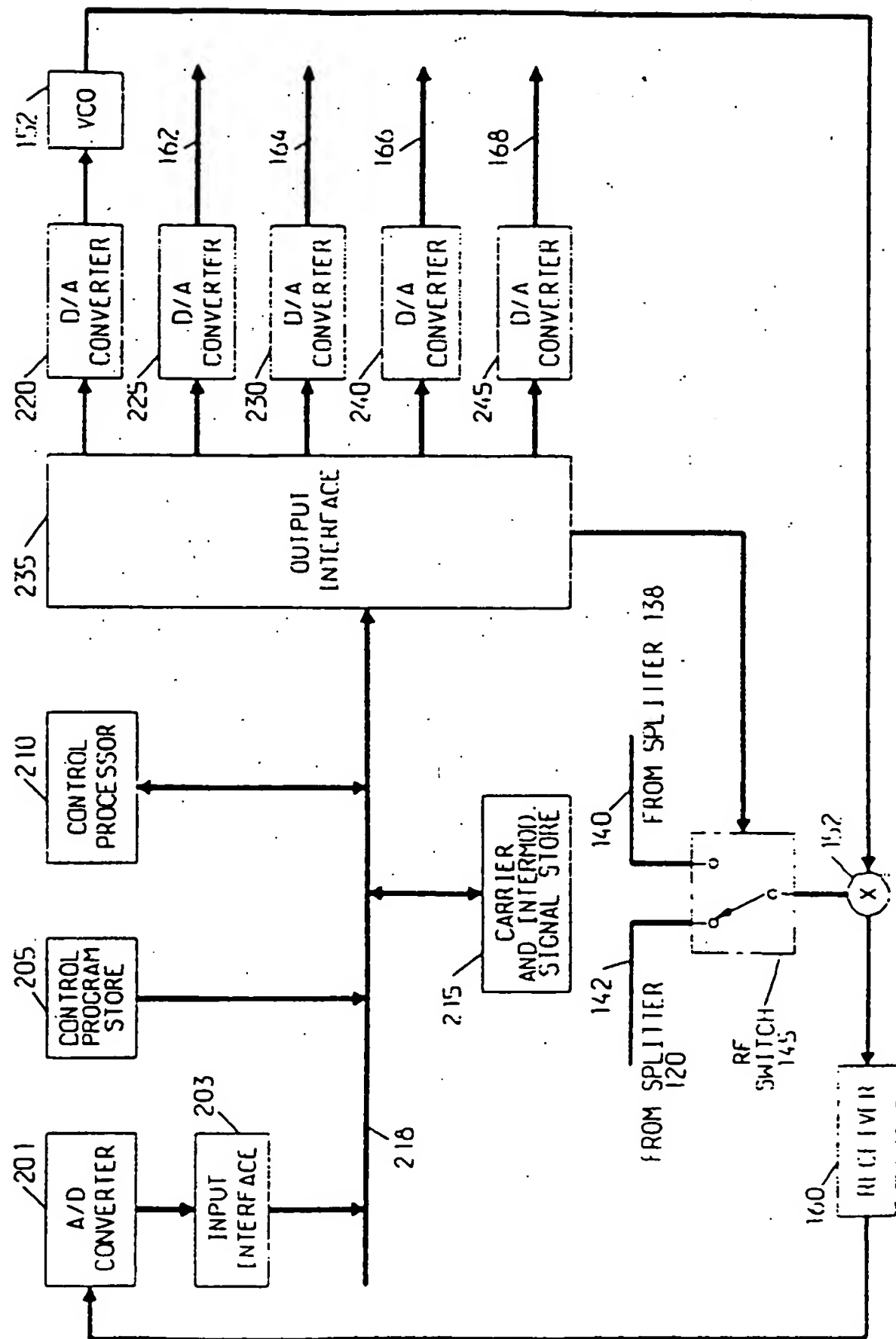


FIG. 3

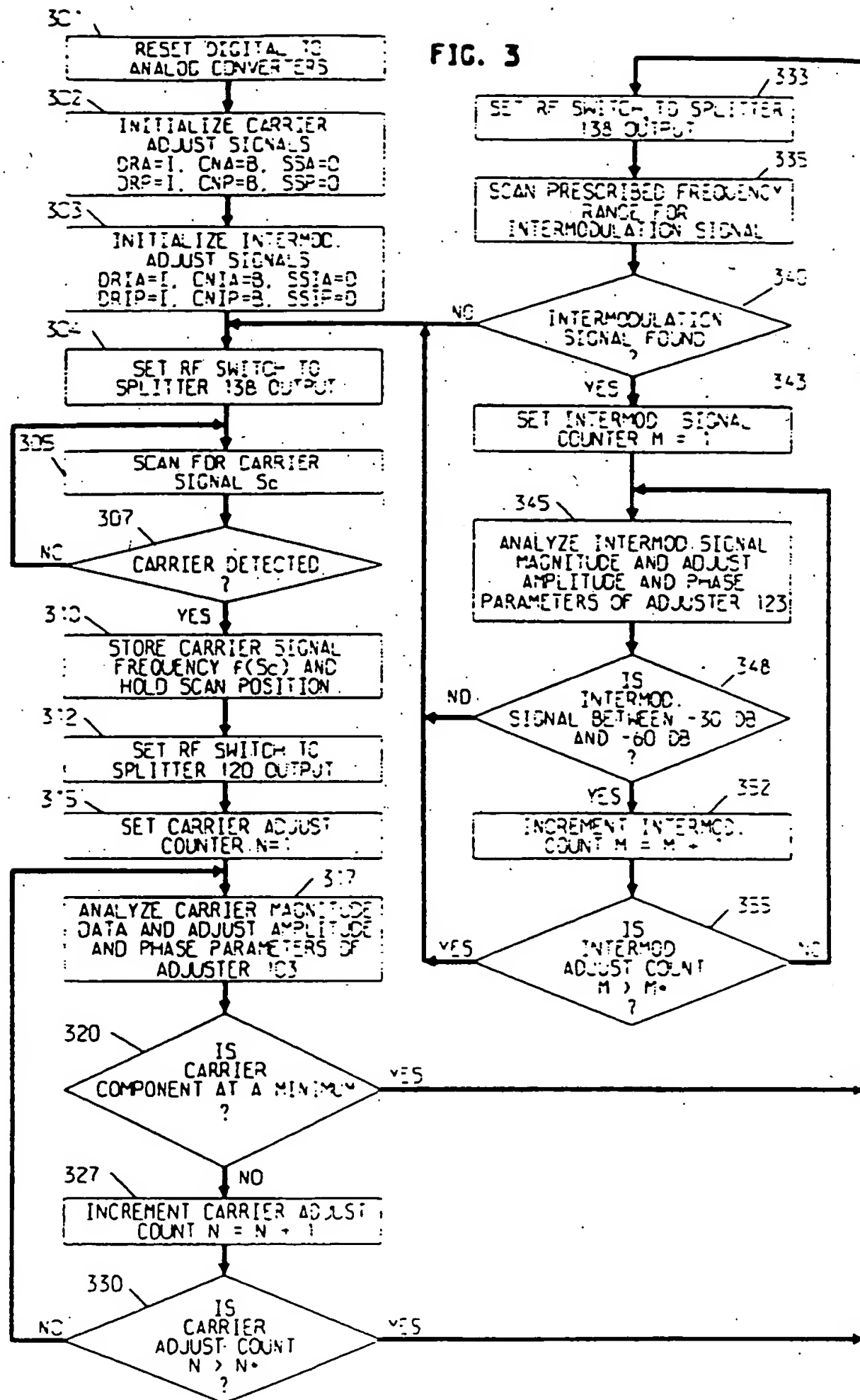


FIG. 4

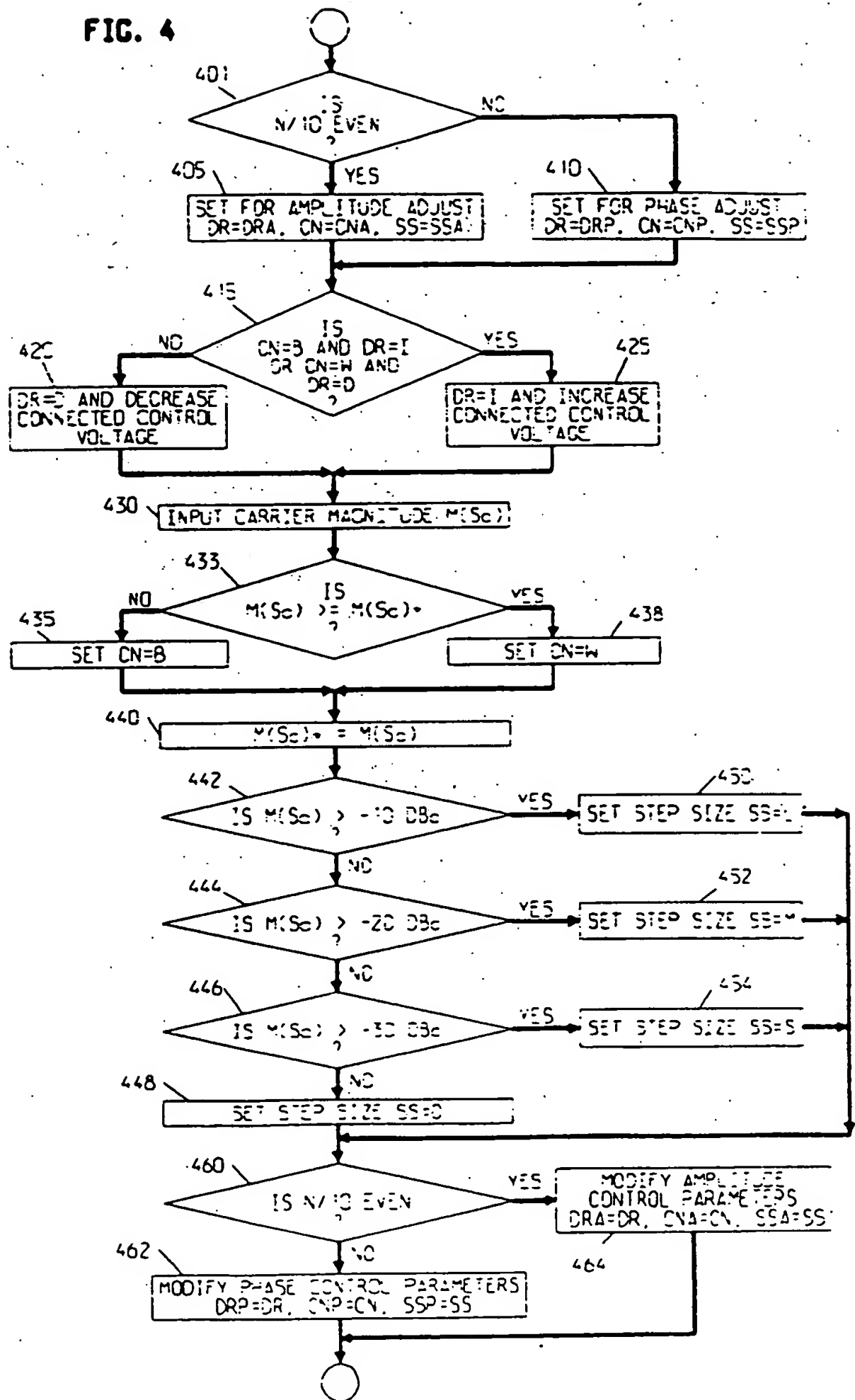


FIG. 5

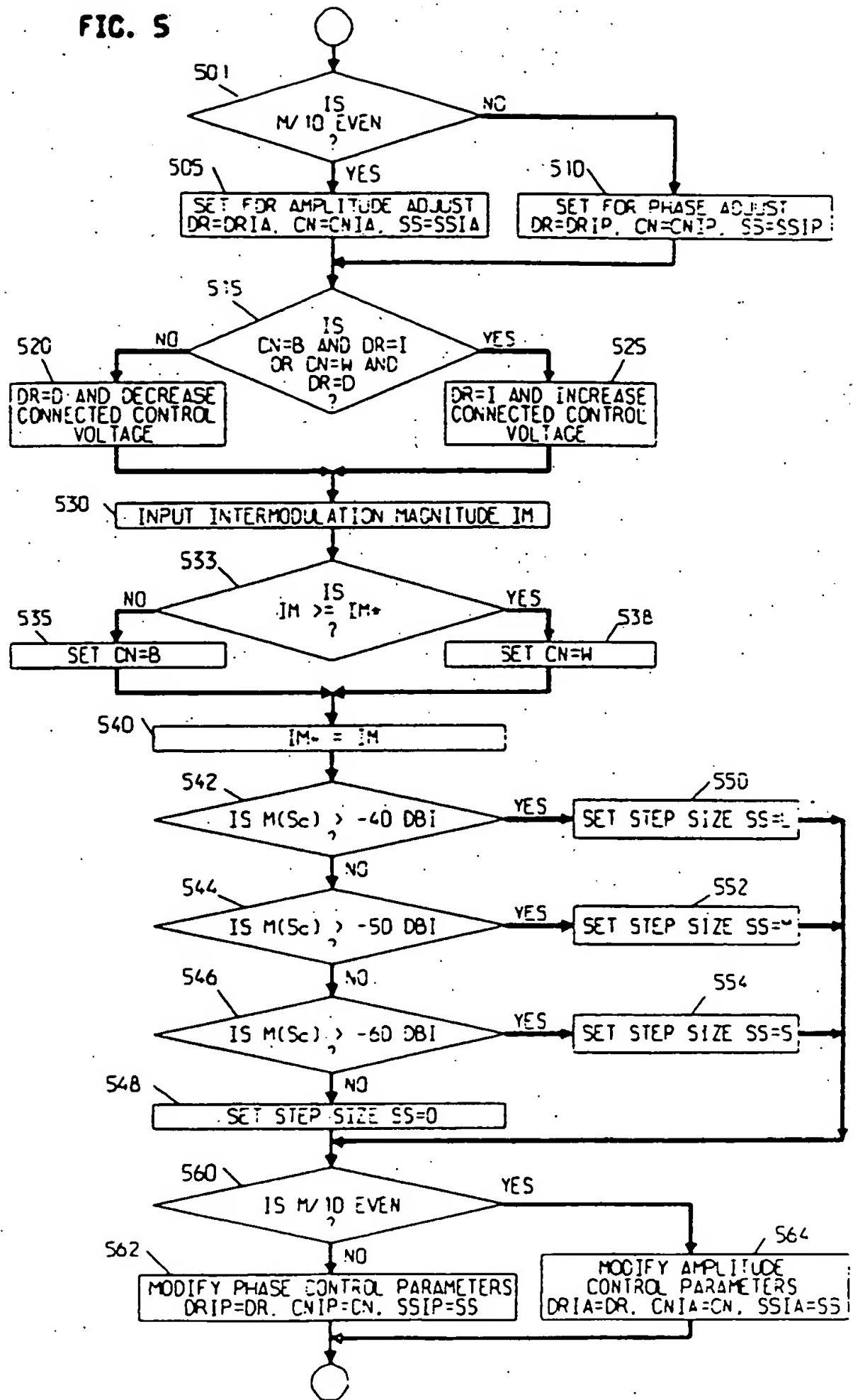


FIG. 6

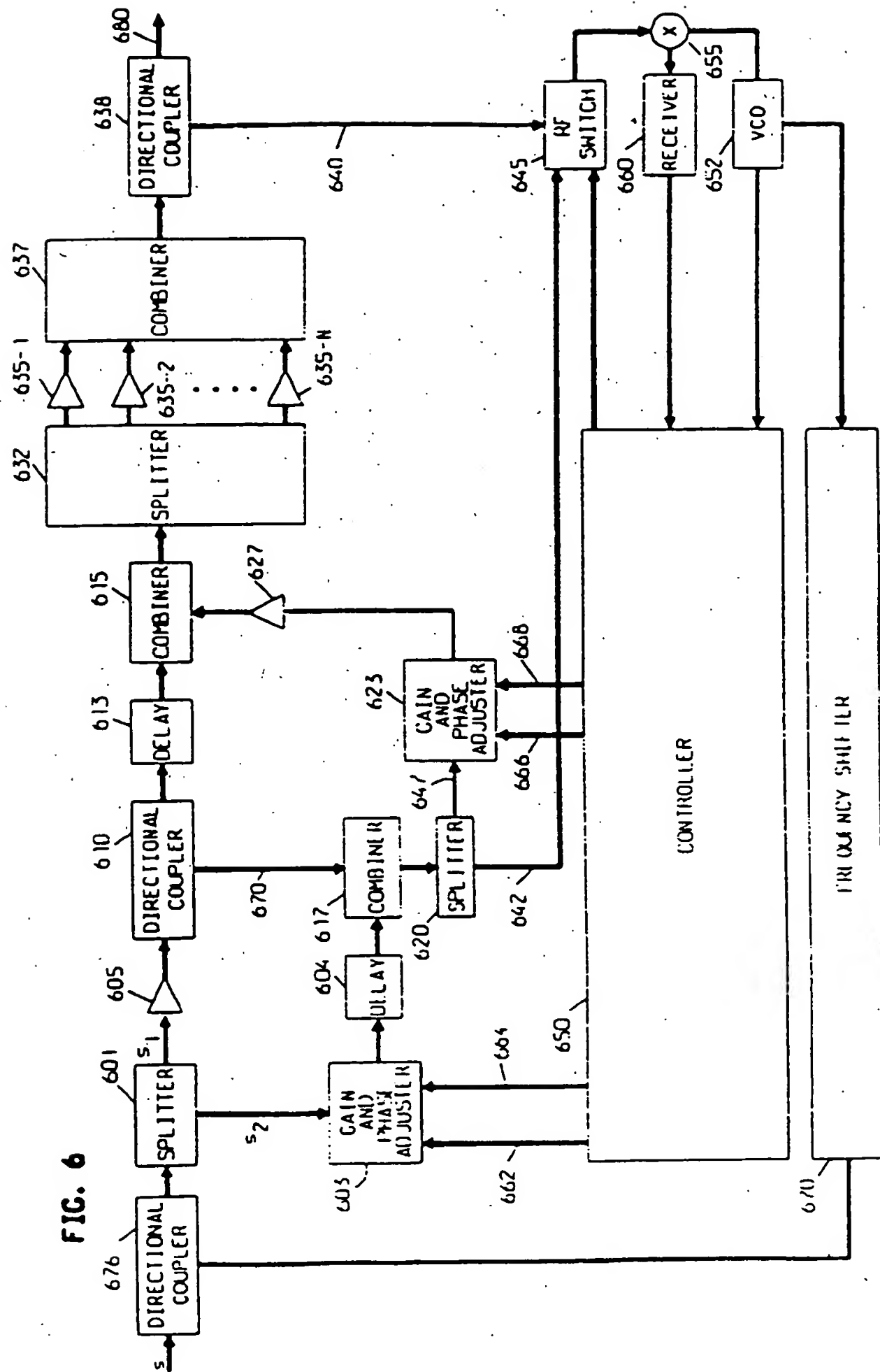


FIG. 7

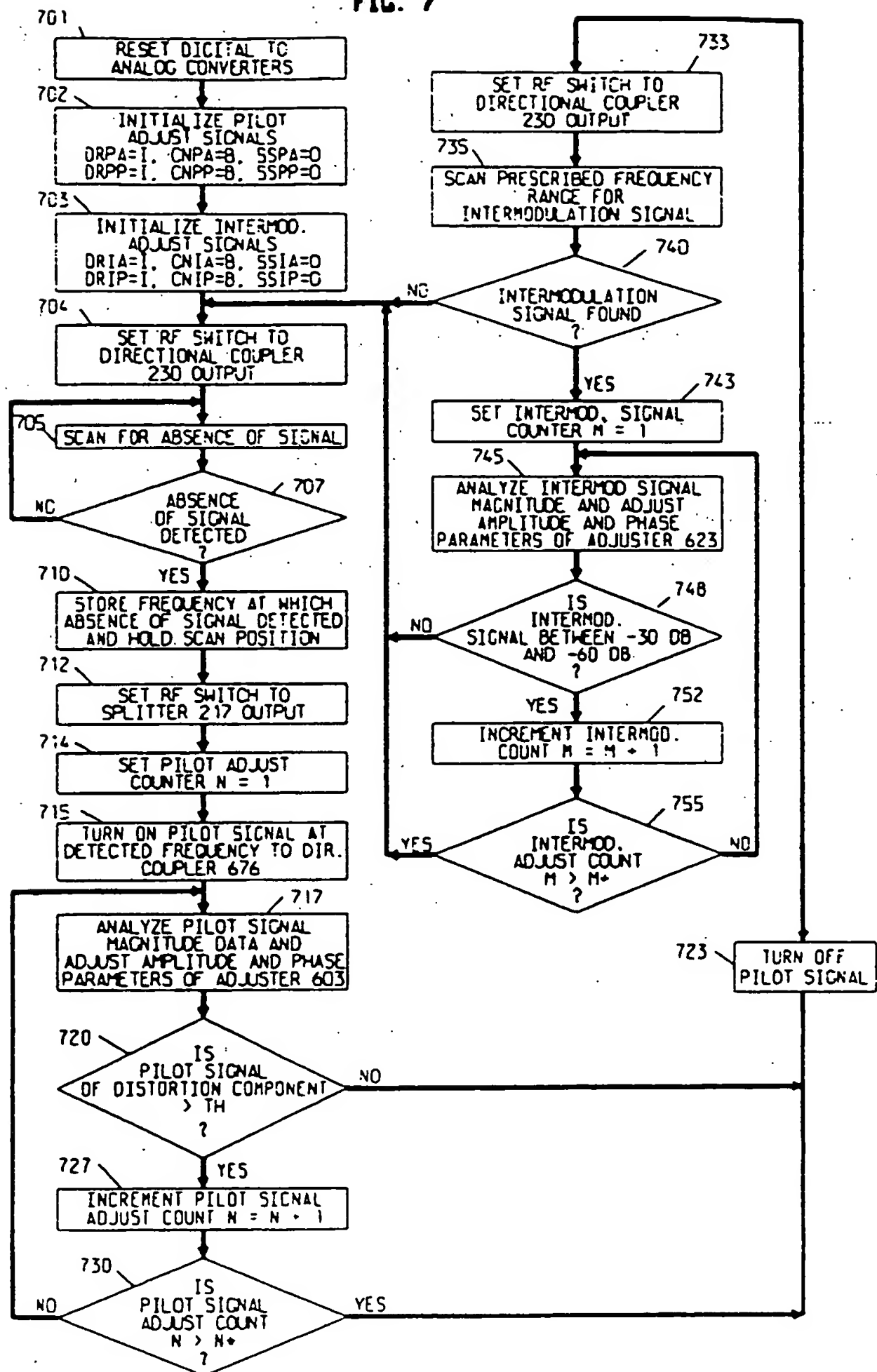


FIG. 8

